

## CLAIMS

What is claimed is:

- 1 1. A digital signal processor, comprising:
  - 2 a content addressable memory (CAM) array having a plurality of rows of
  - 3 CAM cells;
  - 4 an array of storage elements having a plurality of rows of the storage
  - 5 elements coupled to the CAM array, each row of storage elements to store a
  - 6 number corresponding to a data word stored in one of the rows of the CAM cells;
  - 7 and
  - 8 priority logic coupled to the array of storage elements, the priority logic to
  - 9 provide to a plurality of priority signal lines an indication of a location of a
  - 10 particular number in the array of storage elements, wherein the priority logic
  - 11 comprises:
    - 12 a first plurality of compare circuits, each compare circuit coupled to
    - 13 one of the storage elements in the array of storage elements, and each
    - 14 compare circuit having a first input coupled to a storage element, a second
    - 15 input coupled to a match line, and an input/output line coupled to one of
    - 16 the plurality of priority signal lines; and
    - 17 a delay circuit coupled to each of the first plurality of compare
    - 18 circuits.
- 1 2. The digital signal processor of claim 1, wherein the delay circuit comprises
- 2 a multiple tap delay circuit.
- 1 3. The digital signal processor of claim 1, wherein the delay circuit comprises
- 2 a plurality of delay elements, each of the plurality of delay elements coupled to
- 3 one of the plurality of compare circuits.
- 1 4. The digital signal processor of claim 3, wherein each of the delay elements
- 2 is programmable.

1    5.    The digital signal processor of claim 1, wherein each of the compare  
2    circuits comprise a first transistor having a drain coupled to a corresponding  
3    priority signal line and having a gate coupled to a corresponding storage  
4    element.

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1    6.    The digital signal processor of claim 5, wherein the gate of the first  
2    transistor is coupled to the delay circuit through one or more logic gates.

1    7.    The digital signal processor of claim 6, wherein the delay circuit comprises  
2    a plurality of delay elements, each of the plurality of delay elements having an  
3    output coupled to one of the plurality of compare circuits.

1    8.    The digital signal processor of claim 7, wherein the one or more logic  
2    gates comprise a NAND gate having a first input coupled to a corresponding  
3    match line and a having a second input coupled to a corresponding output of  
4    one of the delay elements.

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1    9.    The digital signal processor of claim 8, wherein the NAND gate has an  
2    output and wherein the one or more logic gates further comprise a NOR gate  
3    having a first input coupled the output of the NAND gate, and wherein the NOR  
4    gate has an output coupled to the gate of the first transistor.

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1    10.   The digital signal processor of claim 1, further comprising:  
2              a policy statement table for storing a plurality of policy statements; and  
3              a priority index table for storing a plurality of priority numbers, each  
4              priority number associated with a corresponding policy statement and indicating  
5              the priority of the corresponding policy statement relative to the other policy  
6              statements, wherein the priority index table comprises the priority logic coupled

7 to the policy statement table, wherein the priority logic provides the most  
8 significant priority number to a plurality of priority signal lines.

1 11. The digital signal processor of claim 1, wherein the first plurality of  
2 compare circuits are coupled in a sequence, each of compare circuit having a  
3 third input coupled to a preceding compare circuit in the sequence.

1 12. The digital signal processor of claim 11, wherein each of the compare  
2 circuits comprise a first transistor having a drain coupled to a corresponding  
3 priority signal line and having a gate coupled to a corresponding storage  
4 element, wherein the gate of the first transistor is coupled to the delay circuit  
5 through one or more logic gates.

1 13. The digital signal processor of claim 12, wherein the third input of the  
2 compare circuit is coupled to the one or more logic gates.

1 14. The digital signal processor of claim 13, wherein the one or more logic  
2 gates comprise a first NOR gate having a first input coupled to the third input of  
3 the compare circuit, the first NOR gate having an output coupled to the gate of  
4 the first transistor.

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1 15. The digital signal processor of claim 14, wherein each of the compare  
2 circuits further comprises a second NOR gate having an input coupled to the  
3 gate of the first transistor, the second NOR gate having an output coupled to the  
4 first NOR gate of a succeeding compare circuit in the sequence.

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1 16. A method of operating a digital signal processor, comprising:  
2 resolving a priority line coupled to a first column of compare circuits; and

3 concurrently, de-asserting a match line in the first column of compare  
4 circuits and resolving a next priority line coupled to a second column of compare  
5 circuits.

1 17. The method of claim 16, further comprising de-asserting a match line in  
2 the second column of compare circuits.

1 18. A digital signal processor, comprising:  
2 means for resolving a priority line coupled to a first column of compare  
3 circuits; and  
4 means for concurrently, de-asserting a match line in the first column of  
5 compare circuits and resolving a next priority line coupled to a second column of  
6 compare circuits.

1 19. The digital signal processor of claim 17, further comprising means for de-  
2 asserting a match line in the second column of compare circuits.